AN-1676 LP38512TS-1.8 Evaluation Board

1 Introduction

This board is designed to enable the evaluation of the LP38512TS-1.8 voltage regulator. Each board is assembled and tested in the factory. This evaluation board has the TO-263 5-lead package mounted.

2 General Description

The LP38512 is a linear regulator capable of supplying up to 1.5A of output current, and incorporates Enable and $\overline{\text{Error}}$ flag features.

The device has been designed to work with 10 µF ceramic input and output capacitors. Footprints areas for C_{IN} and C_{OUT} will allow for a variety of sizes.

3 Operation

The input voltage, applied between V_{IN} and GND, should be at least 2.25V, and no higher than 5.5V.

Loads can be connected to V_{OUT} with reference to GND.

Test points are provided on the board to allow monitoring of V_{OUT}, V_{IN}, Enable, and $\overline{\text{ERROR}}$ signals during operation

If the application does not require the Enable function, the EN pin should be connected to directly to the adjacent V_{IN} pin.

4 Enable Operation

The Enable On threshold is typically 1.2V, and typically has 200mV of hysteresis. The voltage signal should rise and fall cleanly, and promptly, through these thresholds.

The Enable pin (EN) has no internal pull-up or pull-down to establish a default condition and, as a result, this pin must be terminated either actively or passively.

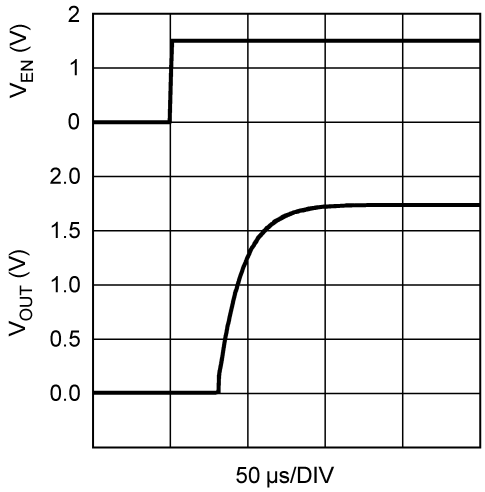

Figure 1. V_{OUT} vs. V_{EN}

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If the Enable pin is driven from a single ended device (such as the collector of a discrete transistor) a pull-up resistor to V_{IN}, or a pull-down resistor to ground, will be required for proper operation. A 1 kΩ to 100 kΩ resistor can be used as the pull-up or pull-down resistor to establish default condition for the EN pin. The resistor value selected should be appropriate to swamp out any leakage in the external single ended device, as well as any stray capacitance.

If the Enable pin is driven from a source that actively pulls high and low (such as a CMOS rail to rail comparator output), the pull-up, or pull-down, resistor is not required.

If the application does not require the Enable function, the EN pin should be connected to directly to the adjacent V_{IN} pin.

The status of the Enable pin also affects the behavior of the $\overline{ERROR}$ Flag. While the Enable pin is high the regulator control loop will be active and the $\overline{ERROR}$ Flag will report the status of the output voltage. When the Enable pin is taken low the regulator control loop is shutdown, the output is turned off, and the internal logic will immediately force the $\overline{ERROR}$ Flag pin low.

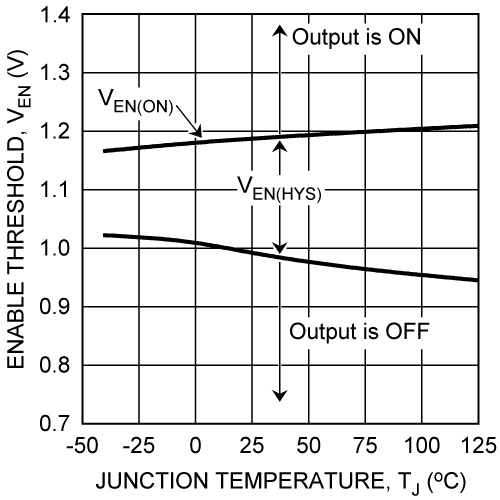

Figure 2. Enable Threshold

5 $\overline{ERROR}$ Flag

When the LP38512 Enable pin is high, the $\overline{ERROR}$ Flag pin will produce a logic low signal when the output drops by more than 10% (typical) from the nominal output voltage. The drop in output voltage may be due to low input voltage, current limiting, or thermal limiting. This flag has a built in hysteresis. The output voltage will need to rise to within 5% of the nominal output voltage for the $\overline{ERROR}$ Flag to return to a logic high state. It should also be noted that when the Enable pin is pulled low, the $\overline{ERROR}$ Flag pin is forced to be low as well.

The internal $\overline{ERROR}$ flag comparator has an open drain output stage. Hence, the $\overline{ERROR}$ pin requires an external pull-up resistor. The value of the pull-up resistor should be in the range of 2 kΩ to 100 kΩ, and should be connected to the LP38512 output voltage pin. The $\overline{ERROR}$ Flag pin should not be pulled-up to any voltage source higher than V_{IN} as current flow through an internal parasitic diode may cause unexpected behavior. When the input voltage is less than typically 1.25V the status of the $\overline{ERROR}$ flag output will not be reliable. The $\overline{ERROR}$ Flag pin must be connected to ground if this function is not used.

The timing diagram in Figure 4 shows the relationship between the $\overline{ERROR}$ flag and the output voltage when the pull-up resistor is connected to the output voltage pin.

The timing diagram in Figure 5 shows the relationship between the $\overline{ERROR}$ flag and the output voltage when the pull-up resistor is connected to the input voltage pin.

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6 Power Dissipation

The TO-263 package alone has a junction to ambient thermal resistance (θ_{JA}) rating of 60°C/W. When mounted on the LP38512TS evaluation board the θ_{JA} rating is approximately 30°C/W.

Although there is only approximately 0.28 square inches of copper area immediately under the tab, the top copper surface area is extended to additional copper area on the bottom of the board by nine thermal vias.

With the 30°C/W thermal rating the LP38512TS evaluation board will deliver the rated 3A output current if V_{IN} = 2.5V, V_{OUT} = 1.8V, and $T_A \leq$ 25°C.

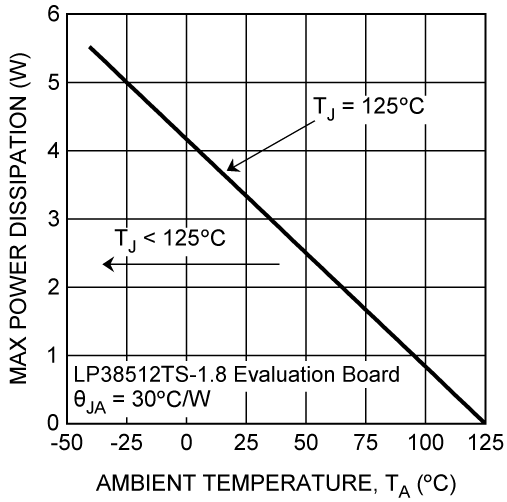

Figure 3. Maximum Power Dissipation vs. Ambient Temperature

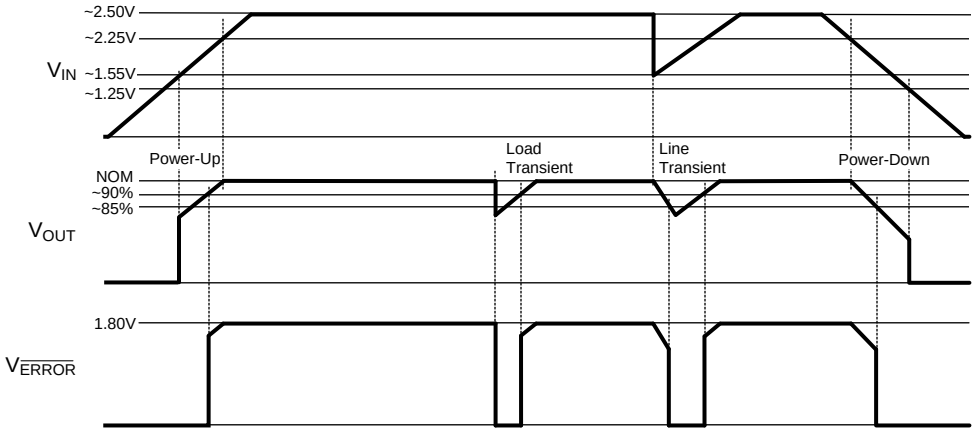

Figure 4. $\overline{\text{ERROR}}$ Flag when Pull-Up is from V_{OUT}

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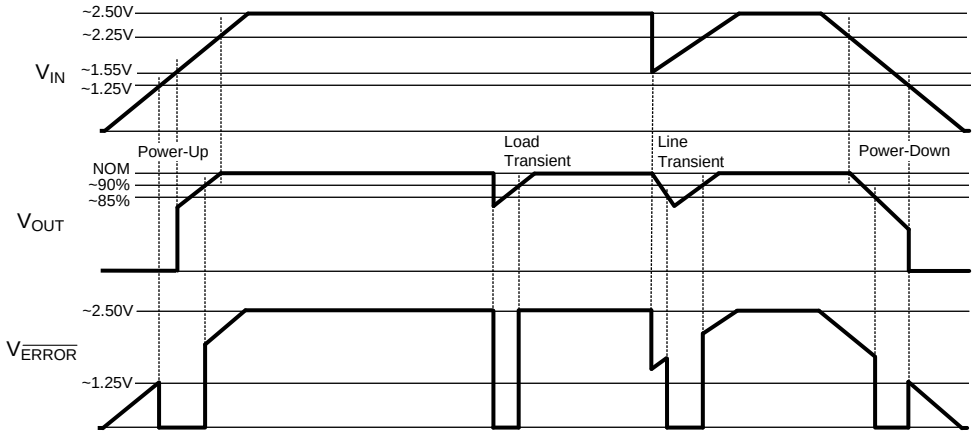
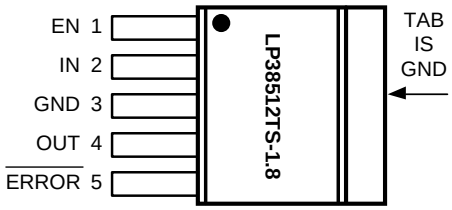


Figure 5. $\overline{\text{ERROR}}$ Flag when Pull-Up is from V_{IN}

7 Connection Diagram



8 Schematic Diagram

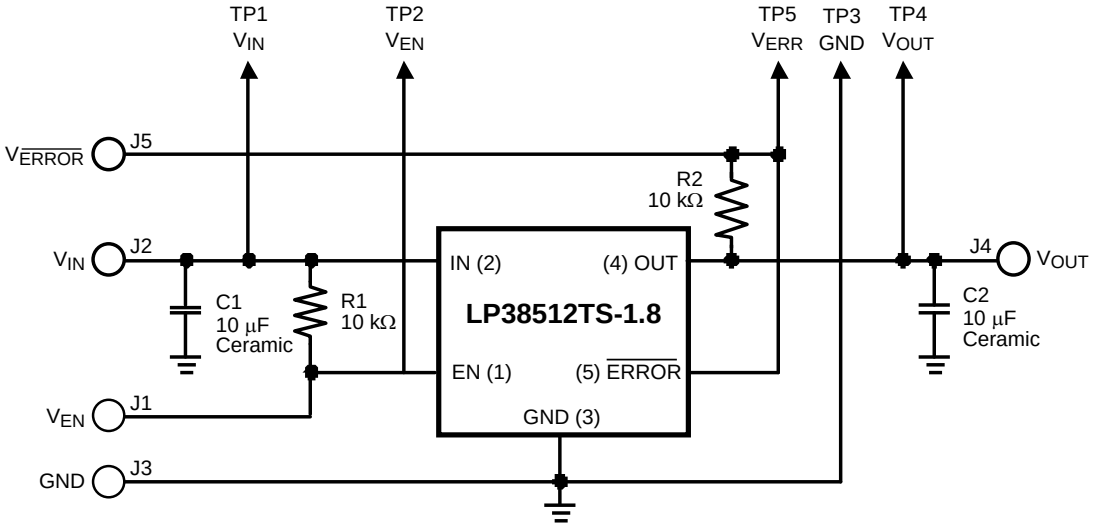


Figure 6. Evaluation Board Schematic

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9 PCB Layout

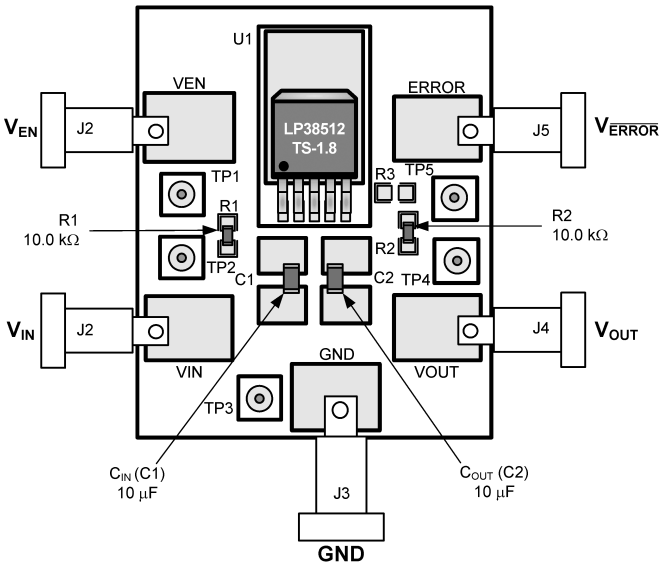

Figure 7. Evaluation Board Component and Pin Layout

10 Bill of Materials

ID	Name	Description	Manufacturer	Part Number
U1	U1	LP38512	Texas Instruments	LP38512
C1	C_{IN}	10 µF, 10%, MLCC, 10V, X7R, 1210	AVX	1210ZC106KAT2A
C2	C_{OUT}	10 µF, 10%, MLCC, 10V, X7R, 1210	AXV	1210ZC106KAT2A
J1	V_{EN}	Banana Jack : Insulated Solder Terminal ; White	Johnson Components	108–0901–001
J2	V_{IN}	Banana Jack : Insulated Solder Terminal ; Red		108–0902–001
J3	GND	Banana Jack : Insulated Solder Terminal ; Black		108–0903–001
J4	V_{OUT}	Banana Jack : Insulated Solder Terminal ; Orange		108–0906–001
J5	V_{ERR}	Banana Jack : Insulated Solder Terminal ; Blue		108–0910–001
R1	—	Resistor: 10 kΩ ±1%; 0805	Vishay Dale	CRCW 0805 1002 F
R2	—	Resistor: 10 kΩ ±1%; 0805	Vishay Dale	CRCW 0805 1002 F
R3	—	Not Installed	N/A	N/A
TP1	TP_{EN}	Turret Terminal : Mounting Hole Diameter = 0.062”	Keystone	1593-2
TP2	TP_{IN}			
TP3	TP_{GND}			
TP4	TP_{OUT}			
TP5	TP_{BIAS}			

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